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10/773,333	02/09/2004	Hiroshi Okumura	Q77321	8920

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SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

EXAMINER	
MONDT, JOHANNES P	
ART UNIT	PAPER NUMBER
3663	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/773,333	OKUMURA, HIROSHI	
	Examiner	Art Unit	
	JOHANNES P. MONDT	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14,16 and 29-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14,16 and 29-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Amendment filed 11/21/08 forms the basis of this Office action. In said Amendment applicant amended the specification, filed a New Sheet for a new Drawing (Figure 11), substantially amended all previously pending claims through substantial amendment of independent claim 29, and added new claim 36. Claims 14, 16 and 29-36 are currently pending and have been examined.

Specification

The following is a quotation from the relevant sections of the Patent Rules under 37 C.F.R. 1.75 that form the basis of the objection made in this office action.

(d)

(1) The claim or claims must conform to the invention as set forth in the remainder of the specification and the terms and phrases used in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description (see §1.58(a)).

2. The Specification is objected to because the limitation "such that a portion of said impurity doping region is not directly below either said second gate electrode or said third gate electrode", as recited in independent claim 29, lines 23-24, although sufficiently evident from Figure 10, should be supported by a written description. Comments on "Remarks" submitted with said Amendment are included below under 'Response to Arguments".

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. ***Claims 29, 16 and 34-36*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant in view Osamu Nakamura (JP 2003-017502A) (made of record by Applicant in IDS filed 6/9/05 and previously cited), Adler et al (5,757,050) (previously cited).

On claim 29: Prior Art as Admitted by Applicant teaches:

a thin film transistor substrate (page 1, Description of the Prior Art and Prior Art Figure 1) comprising:

an insulating substrate 301 (see par. [03]);

a first thin film transistor (driver transistor with gate 304 *capable* of being driven by low voltage) formed above said insulating substrate (cf. Figure 1), comprising a first active layer 302 (island-like portion to the left in Figure 1 comprising 305a; see [03]) formed above said insulating substrate, a first gate insulating film 303 (see [03]) formed on said first active layer and a first gate electrode 304 (see [03]) formed on said first gate insulating film (cf. Figure 1); and

a second thin film transistor (pixel transistor with gate 307 *capable* of being driven by high voltage) formed above said insulating substrate (cf. Figure 1), wherein said second thin film transistor comprises a second active layer 302 (island-like portion of 302 to the right in Figure 1 comprising 305b; see [03]) formed above said insulating substrate, and a second gate insulating film 303/306 (see [03]) formed on said second

active layer, a second gate electrode formed 307 (see [03]) and capable of being driven at high voltage being formed on said second gate insulating film,

wherein said second gate insulating film 303/306 comprises said first gate insulating film 303 (Figure 1) and a gate cover 306 (Figure 1 and [0005]) formed above said first gate insulating film (loc.cit and Figure 1),

wherein said second active layer has at least two impurity doping regions 305b on both sides of the channel ([0005]).

Prior Art as admitted by Applicant does not necessarily teach the further limitations

(a) said "at least two impurity doping regions" are "formed in a self-aligning manner with respect to said first gate electrode" and "so as to overlap said first gate electrode by 0.1 μm or less";

(b) "wherein said second thin film transistor further comprises a third gate electrode driven at low voltage and formed between said second active layer and said second gate electrode with gate length shorter than that of the second gate electrode"; nor

(c) "*wherein said second active layer comprises a first channel region disposed directly below said second gate electrode, a second channel region disposed directly below said third gate electrode and an impurity region disposed between said first and said second channel regions such that a portion of said impurity doping region is not directly below either said second or said third gate electrode*" (i. e., final five (5) lines of independent claim 29), although the Prior Art does discloses said second active layer to comprise a channel layer and two impurity doping regions (401 and 305a, resp.).

With regard to limitation (a), *the limitation "formed in a self-aligning manner with respect to said gate electrode"* only has patentable weight in the result for the final structure and constitutes a product-by-process limitation and is only of patentable weight in as much as the method steps distinguish the final structure, and to the extent not impacting final structure are taken to be product-by-process limitations and non-limiting. A product by process claim is directed to the product per se, no matter how they are actually made. See MPEP 2113, from which it is clear that it is the patentability of the final structure of the product "gleaned" from the process steps that must be determined in a "product-by-process" claim, and not the patentability of the process. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

In the underlying case, forming impurity doping regions in a self-aligning manner is known to strongly reduce the overlap between gate and source/drain regions.

In addition, it would have been obvious to include the limitation "*so as to overlap said first gate electrode by 0.1 μm or less"* in view of Adler et al, who teach a thin film transistor that is self-aligned (col. 2, l. 50-59) and with overlap by 0.1 μm or less (col. 8, l. 24-43). Applicant is reminded that a *prima facie* case of obviousness typically exists when the ranges as claimed overlap the ranges disclosed in the prior art or when the ranges as claimed do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

Furthermore, it would have been obvious to include the further limitation ad (b) in view of Nakamura, who, in a patent document on thin film transistors (hence analogous art) teaches the addition of a third electrode (13 or 23) between an active layer and a gate electrode (17 or 27) with gate/drain overlap so as to improve reliability and achieve low OFF state current (see English abstract). *Motivation* to include the teaching by Nakamura in the Prior Art as admitted by Applicant derives from the advantage of having as low a current as possible when the device is supposed to be off.

Furthermore, gate electrode 17 or 27 by Nakamura et al has a length that exceeds the length of gate electrode 13 (see front Drawing, upper portion, and see Drawing 2, upper portion) and hence the range limitation on gate lengths is met in the Prior Art as cited. A *prima facie* case of obviousness typically exists when the ranges as claimed overlap the ranges disclosed in the prior art or when the ranges as claimed do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties.

Finally, it would have been obvious to include limitation (c) as defined above, in view of Nakamura:

First, it is noted that there is nothing in the inherent properties of an LDD or any other impurity doping region contiguous with a region that is at least during the ON state electrically connecting source and drain precludes it from functioning as a channel region. Examiner thus takes the position that any such region meets “channel region”. *Nakamura* teaches through Drawing 4A and discussion (see computerized translation made of record by examiner, especially paragraphs [0058-[0061]), showing a first

channel region directly below said second gate electrode, which is the gate electrode to the right (i.e., the region marked “P:5E1819/cm3” or, alternatively the sub-region of the domain marked "P:4E17cm3” positioned directly below the second gate electrode, meets the limitation “first channel region”), a second channel region directly below said third gate electrode (marked “B:2E18/cm3”) and an impurity doping region (either the region marked “P:4E17/cm3” or the portion of said region not directly below said second gate electrode), which is also not directly below said third gate electrode). As is clear from Nakamura’s discussion, the invention defined by Figure 4A has proven useful in light of simulation results ([0061]). The invention of Drawing 4A is a variation of the embodiment discussed previously and corresponding to Drawing 2, which discussion is herewith included by reference in its entirety. Again, in particular it is noted that the relative horizontal extent of LDD doping regions, such as the region marked “P:eE17/cm3” in Drawing 4 (see [0058]), is a matter of design (as long as there is some overlap between the LDD region and the second gate electrode (see [0055])), whereby in the case of Drawing 4 the electric field in said LDD region is weakened relative to the field caused by the third gate electrode in the active layer (loc.cit.), thus reducing the hot electron effect further, which provides motivation towards adopting the teaching by Nakamura through the embodiment of Drawing 4. With regard to the particular feature of a non-overlapping portion of LDD region, the discussion of Nakamura as referred to above demonstrates that this feature is a matter of design choice, because both with and without said feature the performance of the TFT substrate is qualified as useful ([0061]). Moreover, the claim would have been obvious because one of ordinary skill

has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. MPEP 2141, section III.

On claim 16: at least one of said impurity doping regions that overlap said second gate electrode includes an LDD structure 14 (see English abstract in Nakamura), which would have been obvious to include in the prior art as admitted by Applicant because LDD regions counteract hot electron effects. *Motivation* to include the teaching on LDD structure by *Nakamura* is the avoidance of hot electron effects in the high-voltage transistor.

On claim 34: said first gate electrode 304, said second gate electrode 307 in the prior art as admitted by applicant are formed under wires which connect to said impurity doping regions 305a and 305b, respectively. Inclusion of the third gate electrode (as shown would have been obvious over Nakamura) necessarily places said gate electrode between the active layer and the second gate electrode according to claim 29 and hence places said third gate electrode also under said wires that connect to said impurity doping regions.

On claim 35: in the combined invention, said impurity doping region 21k between the second gate electrode and the third gate electrode is an LDD region (see Nakamura et al. [0049]-[0051]) (see also rejection of claim 29, in which this is also pointed out).

On claim 36: said first channel region, said second channel region and said impurity doping region are configured in a plane configuration (see Figure 4).

5. ***Claim 14*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant, Nakamura and Adler et al as applied to claim 29 above, and further in view of Zhang et al (6,507,069 B1) (previously cited). As detailed above, claim 29 is unpatentable over Prior Art as admitted by Applicant in view of Nakamura and Adler et al, none of the above references, however, necessarily teaching the further limitation defined by claim 14. However, it would have been obvious to include said further limitation in view of Zhang et al, who, in a patent on thin film transistors, hence analogous art, teach self-aligned thin film transistors to include LDD regions for the specific reason to reduce the OFF current (col. 2, l. 9-15). *Motivation* to include the teaching by Zhang thus derives from the obvious advantage to reduce the inherently unwanted current in the OFF state.

6. ***Claim 30*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant, Nakamura and Adler et al as applied to claim 29, and further in view of Izawa et al (5,053,849) (previously cited).

As detailed above, claim 29 is unpatentable in view of Prior Art as Admitted by Applicant, in view of Nakamura and Adler et al. None of these references necessarily teach the further limitation defined by claim 30. *However, it would have been obvious to include the further limitation in view of Izawa et al*, who, in a patent on overlapping gate/drain gate structures (see title), hence analogous art, teach the overlap to be about 0.2 μm (col. 13, l. 53-66), which overlaps the range as claimed. A *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not

overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

7. ***Claims 31-32*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant, Nakamura, and Adler et al as applied to claim 29, in further view of Numasawa et al (6,048,795) (previously cited). As detailed above, claim 29 is unpatentable over Prior Art as Admitted by Applicant, in view of Nakamura and Adler et al. None of these reference necessarily teach the further limitation defined by claim 31. *However, it would have been obvious to include the further limitation ad (c) in view of Numasawa et al*, who, in a patent on gate electrodes formed in a self-alignment process step with source and drain regions (see Figure 2E and col. 1, l. 17-52), hence analogous art, teach the gate electrode to comprise a two –layer structure including a semiconductor layer 13 (hence claim 32 is also met) and a metal layer 14 (col. 3, l. 25 – col. 4, l. 58). *Motivation* to include the teaching by Numasawa et al in the invention of the Prior Art derives from the advantage of increased electric conductivity of the gate electrode without having to give up the convenience of the self-alignment process step in creating source and drain regions with the gate as mask (col. 1, l. 16-30).

8. ***Claim 33*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant, Nakamura and Adler et al as applied to claim 29 above, and further in view of Suzawa et al (5,914,498) (previously cited).

As detailed above, claim 29 is unpatentable over Prior Art as Admitted by Applicant, in view of Nakamura and Adler et al. None of these references necessarily teach:

(A) the further limitation that said third gate electrode is formed of the same material as said first gate electrode; nor the further limitation;

(B) that said third gate electrode has the same thickness as said first gate electrode. *However, it would have been obvious to include the limitations (A) and (B) in view of Suzawa et al*, who teach gate electrodes displaced substantially laterally from each other to be made of the same material (aluminum 105/106: Figure 1A and col. 5, l. 20-27) and to have the same thickness (as witnessed by the reference to the thickness of the gate electrodes: see col. 14, l. 68 and col. 15, l. 1). Applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416; and, furthermore, that a *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. See MPEP 2144.05[R-5].

Response to Arguments

9. Applicant's arguments filed 11/21/08 have been fully considered but they are not persuasive. The substantial amendment of independent claim 29 has overcome the rejection of record in the previous office action based on the embodiment of Drawing 2 in Nakamura. However, further consideration and search reveals that the further limitation currently introduced, and actually only based on Drawings in the original

specification, in particular Figure 10, is in fact disclosed by Nakamura to be a matter of design choice, and furthermore that Nakamura does teach an embodiment meeting the claim limitation, namely: the embodiment discussed in [0058]-[0061] and depicted in Drawings 4A and 4B (especially 4A is relevant for the newly introduced limitation. The rejection of claim 29 as set forth above is herewith included by reference in its entirety in response to applicant's remarks.

10. Finally, although the new Drawing as filed (Figure 11) is indeed but a combination of Figures 5 and 10, and hence is accepted for clarity, and although original Figure 10 does provide written support for the newly introduced limitations in claim 29, nothing in the original specification including original claims provides a verbal account as complete, written support for said limitation. In particular the existence of a portion of an impurity region located between the first and second channel such that said portion is not directly below either the first or second channel, should be recited per amendment to the specification.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHANNES P. MONDT whose telephone number is (571)272-1919. The examiner can normally be reached on 7:30 - 17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Johannes P Mondt/

Primary Examiner, Art Unit 3663